Program at a Glance

Tuesday, September 24th

Workshop Session 1: Chung-Hsun Lin (Intel)	Grand Ballroom	9:00AM-10:00AM
Workshop Session 2: Steven Hung (Applied Materials)	Grand Ballroom	10:00AM-11:00AM
Workshop Session 3: Philippe Blaise (Silvaco)	Grand Ballroom	11:00AM-12:00AM
Lunch Break	Atrium Room	12:00AM-1:30PM
Workshop Session 4: Ilon Joseph (LLNL)	Grand Ballroom	1:30PM-2:30PM
Workshop Session 5: Yuhao Zhang (CPES)	Grand Ballroom	2:30PM-3:30PM
Workshop Session 6: Norman Chang (ANSYS)	Grand Ballroom	3:30PM-4:30PM

Wednesday, September 25th

Breakfast	Atrium Room	8:00AM-8:45AM
Conference Opening	Grand Ballroom	8:45AM-9:00AM
Plenary Talk I: Barbara De Salvo	Grand Ballroom	9:00AM-9:50AM
Coffee Break	Atrium Room	9:50AM-10:10AM
Breakout Session 1 Invited: Tillmann Kubis General: Process Modeling (4 papers)	Grand Ballroom	**10:10AM-12:00PM**
Breakout Session 2 Invited: Victor Moroz General: Power Devices (3 papers)	Sainte Claire Ballroom	**10:10AM-12:00PM**
Lunch Break	Atrium Room	12:00AM-1:30PM
Breakout Session 3 General: 2D Materials (5 papers)	Grand Ballroom	**1:30PM-3:10PM**
Breakout Session 4 General: First Principles & Transport (5 papers)	Sainte Claire Ballroom	**1:30PM-3:10PM**
Coffee Break	Atrium Room	3:10PM-3:30PM
Poster Session: (HC:120/2x60)	Atrium Room	3:30 PM-5:30PM
Reception	Grand Ballroom	6:00PM-8:00PM

Thursday, September 26th

Event	Location	Time
Breakfast	Atrium Room	8:00AM-8:45AM
Plenary Talk II: Aveek Sarkar	Sainte Claire Ballroom	9:00AM-9:50AM
Coffee Break	Atrium Room	9:50AM-10:10AM
Breakout Session 5 Invited: Souvik Mahapatra General: Ferroelectric Modeling (4 papers)	Grand Ballroom	**10:10AM-12:00PM**
Breakout Session 6 Invited: Denis Rideau General: Sensors & Optoelectronics (4 papers)	Sainte Claire Ballroom	**10:10AM-12:00PM**
Lunch Break	Atrium Room	12:00AM-1:30PM
Breakout Session 7 General: Memory (5 papers)	Grand Ballroom	**1:00PM-2:40PM**
Breakout Session 8 General: Machine Learning/AI-based Modeling (5 papers)	Sainte Claire Ballroom	**1:00PM-2:40PM**
SISPAD Social Event	Pier 39	3:00PM-8:00PM

Friday, September 27th

Event	Location	Time
Breakfast	Atrium Room	8:00AM-8:45AM
Breakout Session 11 Invited: Blanka Magyari-Kope General: Advanced CMOS Logic (3 papers)	Grand Ballroom	**9:00AM-9:50AM**
Breakout Session 12 Invited: Woosung Choi General: Quantum Computing *(3 papers)*	Sainte Claire Ballroom	**9:00AM-9:50AM**
Coffee Break	Atrium Room	10:30AM-10:50AM
Breakout Session 9 General: Planar CMOS (3 papers)	Grand Ballroom	**10:50AM-11:50AM**
Breakout Session 10 General: Packaging Modeling (3 papers)	Sainte Claire Ballroom	**10:50AM-11:50AM**
Lunch Break	Atrium Room	12:00AM-1:30PM
Conference Ends	Grand Ballroom	1:30PM-3:10PM

General Information

Conference Venue

The conference will be held in presence at the The Westin San José located in 302 S Market St, San Jose, California, 95113 (https://maps.app.goo.gl/N81cQgAShFXqKV4v9).

San José

San José is a city located in the heart of Silicon Valley in Northern California, United States. It's the largest city in terms of both population and area within Santa Clara County. San José is known for its thriving tech industry, diverse population, and a blend of urban and suburban landscapes.

How To Reach San José

San José is easily accessible by various modes of transportation due to its location in Silicon Valley, California.

Here are the common ways to reach San José:

By Air:

The most convenient way to reach San José from distant locations is by flying into the Norman Y. Mineta San José International Airport (SJC). It's a major airport serving the city and offers both domestic and limited international flights.

By Car:

If you're traveling within California or nearby states, you can reach San José by car. Major highways that connect to San José include Interstate 280 (I-280), Interstate 680 (I-680), and U.S. Route 101 (US-101).

By Public Transit:

If you're already in the San Francisco Bay Area, you can use the Bay Area Rapid Transit (BART) system to get relatively close to San José and then transfer to the Santa Clara Valley Transportation Authority (VTA) light rail or bus services to reach your final destination within the city.

Breakout Sessions

Wed, September 25th

Breakout Session 1 | Process Modeling

Grand Ballroom | 10:10AM-12:00PM

Invited Talk

10:10AM-10:40AM

Mode space in DFTB quantum transport in the nanodevice simulation tool NEMO5

Logan Melican, Han-Wei Hsiao, Daniel Lemus and Tillmann Kubis

Paper 1.1

10:40AM-11:00AM

MD simulation of epitaxial recrystallization and defect structure of Al-implanted 4H-SiC

Sabine Leroch (University of echnology Vienna), Robert Stella (University of Technology Vienna), Andreas Hössinger (Silvaco Europe Ltd.) and Lado Filipovic (University of Technology Vienna)

Abstract

The 4H-SiC structure is highly technologically relevant because of its good thermal conductivity, the high electric field breakdown strength, and the widest band gap of 3.26 eV among the alternative SiC polytypes. Thus, it plays a major role in semiconductor fabrication. The as-implanted amorphous 4H-SiC structure was produced by high dose Al implantation at room temperature in our previous molecular dynamics (MD) study. To provide a large number of carriers in the bnd gap the Al dopants must occupy Si-lattice sites in a nearly defect-free 4H-SiC crystal. To reduce the number of defects and to recrystallize the as-implanted SiC, thermal annealing was done at temperatures ranging from 1000 to 2150 K. We investigated the basic mechanisms for recrystallization such as expitaxial regrowth as well as the role of the Al dopant in this process in dependence of temperature and time in comparison to experiments. Where we could show that the general physical behavior of the system is maintained in the MD simulation. Moreover, we discussed the remaining defect structure consisting of single point defects, defect complexes and small defect clusters after high temperature annealing.

Paper 1.2

11:00AM-11:20AM

Generalization of Fick's law and derivation of interface segregation parameters using microscopic atomic movements

Chihak Ahn (Samsung semiconductor Inc.), Joohyun Jeon (Samsung Electronics), Seungmin Lee (Samsung Electronics), Woosung Choi (Samsung Semiconductor Inc.), Dae Sin Kim (Samsung Electronics.), and Nick Cowern (Newcastle University)

Abstract

Using a microscopic picture of atomic movement we rederived the Fick's diffusion flux equation which naturally includes all types of drift terms (e.g. electrical drift, stress driven movement, and binding energy related effects). With a similar method, two phase segregation transfer rate and three phase segregation trapping/emission rates are also defined with measurable or calculable quantities.

Paper 1.3

11:20AM-11:40AM

Identification of key atomic process of Nickel induced crystallization from First-principles Calculations

Yutaro Ogawa (Advanced Memory Development Center, Memory Division, Kioxia Corporation), Hikari Suzuki (Core Technology Research Center, Frontier Technology R&D Institute, Kioxia Corporation), and Masayasu Miyata (Advanced Memory Development Center, Memory Division, Kioxia Corporation)

Abstract

In order to improve the efficiency of metal-induced lateral crystallization (MILC) using Ni, it is important to understand the fundamental mechanisms. In this study, the NiSi2/amorphous Si (a-Si) interface is appropriately modeled and the atom transfer behavior during the MILC process was explored by first-principles calculations. It is found that the overall picture of MILC mechanism can be effectively comprehended through three fundamental processes: (1) the formation of Ni vacancies at the a-Si interface, (2) the diffusion of Ni vacancies within the bulk NiSi2, and (3) the reconstruction of the c-Si interface. The trends under stress, observed in experiments, are explained by applying this mechanism to the MILC process.

Paper 1.4

11:40AM-12:00PM

Modeling Non-Uniformity During Two-Step Dry Etching of Si/SiGe Stacks for Gate-All-Around FETs

Ziyi Hu (Institute of Microelectronics, Chinese Academy of Sciences), Lado Filipovic (CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors, Institute for Microelectronics, TU Wien), Junjie Li (Institute of Microelectronics, Chinese Academy of Sciences), Lingfei Wang (Institute of Microelectronics, Chinese Academy of Sciences), Zhicheng Wu (Institute of Microelectronics, Chinese Academy of Sciences), Rui Chen (Institute of Microelectronics, Chinese Academy of Sciences), Yayi Wei (Institute of Microelectronics, Chinese Academy of Sciences) and Ling Li (Institute of Microelectronics, Chinese Academy of Sciences).

Abstract

As advanced-node semiconductor devices scaled down and more electrostatic control over the channel became essential, the gate-all-around field-effect transistor (GAAFET) became the go-to geometry to take over after the FinFET. GAAFET devices achieve longer effective channels by providing access to multiple channel pathways and by introducing strain in the channel. One of the most critical steps in GAAFET fabrication is the selective lateral etching of the SiGe layers, which is the basis for the formation of an inner-spacer.

The difficulty of selective SiGe etching is ensuring high control over the lateral depth and shape of the SiGe layer while minimizing Si layer loss. Existing studies show that there is a non-uniform profile on the substrate surface during wet or dry selective etching of SiGe, which cannot be modeled using standard process TCAD (Technology Computer Aided Design) approaches.

In this paper, we propose a method for the continuous simulation of the two-step dry etching process – anisotropic etching of the Si/SiGe stack and subsequent isotropic selective etching of SiGe – to study the mechanism behind the non-uniform profile formation. The proposed method is able to simulate the non-uniform profile accurately, which was calibrated and verified with experimental data.

Breakout Session 2 | Power Devices

Sainte Claire Ballroom | 10:10AM-12:00PM

Invited Talk
Logic DTCO/STCO

10:10AM-10:40AM

Victor Moroz, Synopsys Inc.

Paper 2.1

10:40AM-11:00AM

Simulating Terahertz Plasma Oscillations in Transistors

Ashwin Tunga (University of Illinois Urbana-Champaign), Michael Shur (Rensselaer Polytechnic Institute), Matt Grupen (Air Force Research Laboratory Sensors Directorate), David Hill (SRI International), and Shaloo Rakheja (University of Illinois Urbana-Champaign)

Abstract

Terahertz plasma oscillations in GaN HEMTs are simulated in a TCAD environment using the Fermi kinetics transport model. Parallels are drawn between the Boltzmann transport equation and the shallow water dynamics used in previous studies to explain the oscillations. The necessary simulation conditions needed to observe the oscillations in a TCAD environment are described. Further discussion on the significance of the average momentum relaxation time and the rationale for choosing its value is presented. Transient simulations of THz oscillations are demonstrated when the gate voltage is perturbed at the quiescent point. A physical theory of the plasma oscillations is proposed by analyzing the oscillations in channel electron concentration, electron temperature and electric field with time. The electron temperature and electric field profiles are observed to be out of phase with each other, alluding to the fact that the energy is exchanged back and forth between the hot electrons and the EM fields, leading to the plasma oscillations.

Paper 2.2

11:00AM-11:20AM

Novel Mobility Enhancement Schemes for Next Generation Silicon Carbide (SiC) Trench MOSFET Technology

Pratik B Vyas (Applied Materials Inc.), Ashish Pal (Applied Materials Inc.), Stephen Weeks (Applied Materials Inc.), Joshua Holt (Applied Materials Inc.), Archana Kumar (Applied Materials Inc.), Lucien Date (Applied Materials Inc.), Ludovico Megalini (Applied Materials Inc.), Michel Khoury (Applied Materials Inc.), Durga Chaturvedula (Applied Materials Inc.), Michael Chudzik (Applied Materials Inc.), Siddarth Krishnan (Applied Materials Inc.), Subi Kengeri (Applied Materials Inc.) and El Mehdi Bazizi (Applied Materials Inc.)

Abstract

New mobility improvement solutions are proposed for next generation SiC trench MOSFET with higher aspect ratio trenches. A combination of channel counter-implant and pocket implant is shown to be most effective for improving mobility without VT loss. Using our proposed integration scheme and calibrated modeling, we project an 80% improvement in mobility and 40% improvement in channel resistance, realizing the true potential of trench MOSFET architecture for next generation SiC power device technology.

Paper 2.3 11:20AM-11:40AM

Cluster-based semi-empirical model for dopant activation in silicon carbide

(Institute for Microelectronics, TU Wien), Sabine Leroch (Institute for Microelectronics, TU Wien), Andreas Hössinger (Silvaco Europe Ltd) and Lado Filipovic (Institute for Microelectronics, TU Wien).

Abstract

We present a cluster-based semi-empirical model for dopant activation in silicon carbide. We model the following species: dopants on lattice points, point defects, dopant-defect pairs, and small clusters of different sizes. We define the possible reactions between these species, add their reaction kinetics, and use a system of ordinary differential equations to model the time evolution of the concentration of the different species during annealing. We use the MaxLIPO+TR optimizer to obtain the post-implant conditions of the SiC film, including the various cluster concentrations. These concentrations are not measurable and can only be calculated through time-intensive atomistic simulations, which we apply to verify and calibrate our model. Our work gives a practical solution to predict as-implanted defect concentrations, which is missing from previous works.

Breakout Session 3 | 2D Materials

Grand Ballroom | 1:30PM-3:10PM

Paper 3.1 1:30PM-1:50PM

Towards Low Contact Resistance Metal-Transition Metal Dichalcogenide Contacts – A Quantum Transport Study

Pranay Kumar Reddy Baikadi (The University of Texas at Dallas), Raseong Kim (Components Research, Intel Corporation), Peter Reyntjens (KU Leuven), Ashish Verma Penumatcha (Components Research, Intel Corporation), Maarten Van de Put (Imec, Leuven), and William Vandenberghe (The University of Texas at Dallas)

Abstract

In this study, we use Non-Equilibrium Green's Function (NEGF) based quantum transport simulations to investigate metal-Transition-Metal Dichalcogenide (TMD) top contacts. Using MoS2 as an example TMD, we explore the impact of the surrounding dielectric and spatially non-uniform doping on contact resistance (Rc), while accounting for image-force barrier lowering (IFBL). We find that a low-κ top dielectric is crucial in reducing the tunneling width (TW) for the electrons and thus Rc. We also find that heavily doping the MoS2 layer underneath the metal has an insignificant effect in terms of reducing TW and Rc.

Paper 3.2 1:50PM-2:10PM

Contact Resistance in Monolayer MoS2 Edge-Contacts: "Electrostatic" vs Substitutional doping

Madhuchhanda Brahma (University of Texas at Dallas), Maarten L. Van de Put (University of Texas at Dallas), Edward Chen (Taiwan Semiconductor Manufacturing Company (TSMC)), Massimo V. Fischetti (University of Texas at Dallas), and William G. Vandenberghe (University of Texas at Dallas)

Abstract

Two-dimensional materials, owing to their unique structure and electronic properties, have emerged as alternative channel materials to Silicon to extend the CMOS scaling beyond the Moore's Law projection. However, a severe

bottleneck that negates most of the advantages and prohibits these materials from practical industrial application: high contact resistance, primarily due to the presence of a high Schottky barrier at the interface with metal contacts. While some theoretical studies have examined the 2D material contacts, focusing on simplified models excluding Schottky barrier junction [1] or study of the interface chemistry and extraction of Schottky barrier height [2-3], and ab initio quantum transport simulation of the carrier injection methods [2-4], the influence of surrounding dielectric and image force barrier lowering, computationally difficult in density functional theory (DFT) studies, has been rarely investigated. Recent studies have highlighted the significant impact of surrounding dielectrics on contact resistance of 2D materials, indicating the importance of a low-dielectric environment for achieving low-resistance contacts [5-8]. In our most recent work, we showed that, in addition to degenerately doping the channel, a low-κ dielectric environment is favorable for achieving low resistance contacts, with its effect being more pronounced than the interface coupling strength of the 2D material edge contacts [6].

While substitutional doping [9] often leads to heavily doped 2D materials with accompanying lattice and surface defects, "electrostatic" doping [10], i.e. modulating charge carriers by back-gate bias, offers a non-destructive alternative. In this paper, we develop a model to calculate transmission through metal-2D edge-contact configurations, incorporating effects of surrounding dielectric and back-gate bias and compare the contact resistance in substitutionally doped contacts with "electrostatically" doped ones. For substitutionally doped contacts without gate bias, we considered infinitely thick top and bottom oxides, while for "electrostatically" doped edge contacts, we selected a bottom oxide of finite thickness. We consider various structures (shown schematically in Fig. 1) of monolayer molybdenum disulfide (MoS2) edge-contact, and utilize band structure from DFT calculations and the Wentzel–Kramers–Brillouin (WKB) approximation to calculate the transmission probabilities through the Schottky barrier [6]. Numerical solutions to Poisson's equation provide the electrostatic potential within the 2D semiconductor, while analytical methods account for image-force barrier lowering [6]. Our results (Fig. 2) indicate that in "electrostatically" doped edge-contacts, low-κ top and bottom insulators result in low-contact resistance The image-force barrier-lowering in edge-contacts at distances much larger than the 2D layer thickness, is determined by the back-gate bias (Fig. 3) , whereas in substitutionally doped contacts, it is controlled by the dielectric permittivity of the surrounding oxide and the TMD [6]. Additionally, we observed that in all cases, "electrostatically" doped devices exhibit worse contact resistance than substitutionally doped ones, and only very high gate bias, such as > 1V, can yield sufficiently low contact resistance when using a high- κ back gate oxide.

Paper 3.3

2:10PM-2:30PM

Efficient Quantum Simulations of Devices Based on 2D Materials Including Vertical Heterojunctions

Alfonso Sanchez-Soares (EOLAS Designs), Thomas Kelly (EOLAS Designs), Sheng-Kai Su (Taiwan Semiconductor Manufacturing Company), Edward Chen (Taiwan Semiconductor Manufacturing Company), James C Greer (University of Nottingham Ningbo China) and Giorgos Fagas (Tyndall National Institute, University College Cork).

Abstract

We present a modelling framework that enables efficient exploration of the electrical performance of devices based on 2D material heterojunctions. Electronic structure data from density functional theory (DFT) simulations is used to extract parameter for k.p Hamiltonians. Material models are then employed in device simulations based on non-equilibrium Green's functions (NEGF) for a quantum-mechanical description of charge transport. Electron-phonon scattering is included in order to account for dissipative phenomena as well as phonon-assisted interlayer charge transport. We demonstrate our methodology with an application on a Dirac-source field-effect transistor (DS-FET) based on a monolayer MoS2 channel (ML-MoS2) with a graphene contact.

Paper 3.4 2:30PM-2:50PM

First-principles study of the origins of random telegraph noise in MoS2/hBN-based field-effect transistors

Ryong-Gyu Lee (Korea Advanced Institute of Science & Technology (KAIST)), Jiyoon Song (Korea Advanced Institute of Science & Technology (KAIST)) and Yong-Hoon Kim (Korea Advanced Institute of Science & Technology (KAIST)).

Abstract

In the development of nanoscale field-effect transistor (FET) devices, defects in the gate dielectric are becoming a more critical factor for device reliability. However, the atomistic understanding of the instabilities in threshold voltage such as bias-temperature instabilities, 1/f noise, and random telegraph noise (RTN) remains limited. Herein, we describe our effort in establishing first-principles theoretical tools for the analysis of RTN. We consider hexagonal boron nitride (hBN)-encapsulated MoS2-based 2D FETs, with various defect candidates introduced in the hBN layer. Based on the multi-space constrained-search density functional theory framework, we study the defect energetics under different temperature and gate-bias conditions. Mapping to the non-radiative multi-phonon model, configuration coordinate diagram analyses provide the classical activation barriers for defect trapping/de-trapping behaviors and capture and emission times for RTN. Our results reveal that both hBN CB and VN defects can contribute to fast and slow RTNs for the MoS2 FET, respectively.

Paper 3.5 2:50PM-3:10PM

Switching Behavior of Graphene Nanoribbon FETs

Mathias Pech (TU Dortmund) and Dirk Schulz (Technical University Dortmund)

Abstract

An efficient model capable of the time-resolved modeling of armchair graphene nanoribbon field-effect transistors based on a Wigner Transport Equation with non-parabolic corrections is presented. With the inclusion of a mode-space approach the computational burden is heavily reduced. The resulting charge carrier and current densities agree well with those obtained through a real space tight-binding formulation of a non-equilibrium Greens Function method in the stationary case. The self-consistent and transient capabilities of our proposed approach are demonstrated for the THz switching behavior. Furthermore, the presented method is well suited for the analysis of nanotubes or nanoribbons composed of different materials, as well as for the extension to interband transport.

Breakout Session 4 | First Principles & Transport

Sainte Claire Ballroom | 1:30PM-3:10PM

Paper 4.1 1:30PM-1:50PM

Band alignment in GAA nanosheet structures from density dependent hybrid functional and many-body GW methods

Troels Markussen (Synopsys Denmark), Rasmus Faber (Synopsys Denmark), Petr Khomyakov (Synopsys Denmark), Brecht Verstichel (Synopsys Denmark) and Anders Blom (Synopsys Inc).

Abstract

In the development of nanoscale field-effect transistor (FET) devices, defects in the gate dielectric are becoming a

more critical factor for device reliability. However, the atomistic understanding of the instabilities in threshold voltage such as bias-temperature instabilities, 1/f noise, and random telegraph noise (RTN) remains limited. Herein, we describe our effort in establishing first-principles theoretical tools for the analysis of RTN. We consider hexagonal boron nitride (hBN)-encapsulated MoS2-based 2D FETs, with various defect candidates introduced in the hBN layer. Based on the multi-space constrained-search density functional theory framework, we study the defect energetics under different temperature and gate-bias conditions. Mapping to the non-radiative multi-phonon model, configuration coordinate diagram analyses provide the classical activation barriers for defect trapping/de-trapping behaviors and capture and emission times for RTN. Our results reveal that both hBN CB and VN defects can contribute to fast and slow RTNs for the MoS2 FET, respectively.

Paper 4.2 — 1:50PM-2:10PM

Cation Disorder Limited IGZO Mobility Calculation Based on the Density Functional Theory

Seung Hyo Han (Korea Advanced Institute of Science and Technology), Deokhwa Seo (Korea Advanced Institute of Science and Technology), Jun-Hwe Cha (R&D Division, SK hynix Inc.), Seiyon Kim (R&D Division, SK hynix Inc.) and Mincheol Shin (Korea Advanced Institute of Science and Technology)

Abstract

In this work, we present a density functional theory (DFT) based method to calculate the electrical properties of crystalline IGZO channel material. The cation disorder limited mobilities of crystalline IGZO with various composition ratios are calculated by directly utilizing DFT-generated samples and their Hamiltonians, and results in good agreement with experimental data are obtained. Furthermore, a model Hamiltonian is introduced to perform calculations for larger sized devices. Our method enables rigorous and efficient evaluation of electrical properties for IGZO of various compositions, covering both Zn-rich and In-rich cases.

Paper 4.3 — 2:10PM-2:30PM

Tunneling quantum correction potential model for drift-diffusion simulations of Schottky contact resistance

Anhtuan Pham (Samsung), Mohammad Ali Pourghaderi (Samsung) and Seonghoon Jin (Samsung)

Abstract

A new approach based on tunneling quantum correction potential is proposed for Schottky contact resistance simulation. The TVqc model relies on a quantum correction potential retaining the CBE near the Schottky interface while avoiding non-local mesh and WKB computation for direct tunneling treatment. The TVqc model can be implemented into the DD solver in a straightforward manner. For typical IV characteristic simulations, the TVqc method is faster than the NLT method by 3-4 times while the accuracy remains unchanged.

Paper 4.4 — 2:30PM-2:50PM

AC Quantum Transport Simulation Including Electron-Phonon Scattering

Phil-Hun Ahn (Gwangju Institute of Science and Technology) and Sung-Min Hong (Gwangju Institute of Science and Technology)

Abstract

For the first time, we report the small-signal (AC) nonequilibrium Green function (NEGF) simulation results for an extremely scaled MOSFET, including the electron-phonon scattering. In this work, both the AC Poisson equation and the AC NEGF equations are consistently considered by solving a coupled system of equations. The conservation of the AC currents is checked.

Paper 4.5 — 2:50PM-3:10PM

Electron-Electron Scattering in Non-Parabolic Transport Models

Josef Gull (TU Vienna, Istitute for Microelectronics), Lado Filipovic (TU Vienna, Istitute for Microelectronics) and Hans Kosina (TU Vienna, Istitute for Microelectronics)

Abstract

A two-particle Monte Carlo (MC) algorithm has been developed recently which treats electron-electron scattering (EES) as an ordinary scattering mechanism. In this work, we present the extension of the algorithm to non-parabolic bands, and discuss a statistical enhancement algorithm.

Thu, September 26th

Breakout Session 5 | Ferroelectric Modeling — Grand Ballroom | 10:10AM-12:00PM

Invited Talk — 10:10AM-10:40AM

A TCAD to SPICE Simulation Framework for Analysis of Device to Circuit BTI and HCD Aging

Payel Chatterjee, Karansingh Thakor and Souvik Mahapatra

Paper 5.1 — 10:40AM-11:00AM

Memory Window and Variability Modeling of Multi-Domain Al:HfO2 Ferroelectric NAND Memory

Kuan-Hung Liu (Synopsys Taiwan), Tue Gunst (Synopsys Denmark), Ko-Hsin Lee (Synopsys Taiwan), Anders Blom (Synopsys Inc.) and Xi-Wei Lin (Synopsys Inc.)

Abstract

This paper presents simulation of a three-dimensional ferroelectric NAND memory using a multi-domain Ginzburg–Landau–Khalatnikov polarization model. The model parameters with a variation range following a Gaussian

function are calibrated based on experimental polarization-electric field hysteresis for undoped and 5 mol% Al-doped HfO_2 thin films. The allowed memory window between program and erase states can be enlarged from 2.9 to 12.6V through the incorporation of Al dopant in HfO_2. This polarization enhancement by substituting Hf with Al atom is also justified through atomistic simulation.

Paper 5.2

11:00AM-11:20AM

First-Principles Calculations of Non-Equilibrium Energetics and Polarization Switching in Oxide Ferroelectric Tunnel Junctions

Kaptansinh Rajput (Korea Advanced Institute of Science and Technology (KAIST)), Ryong Gyu Lee (Korea Advanced Institute of Science and Technology (KAIST)), Tae Hyung Kim (Korea Advanced Institute of Science and Technology (KAIST)), Hyeonwoo Yeo (Korea Advanced Institute of Science and Technology (KAIST)) and Yong-Hoon Kim (Korea Advanced Institute of Science and Technology (KAIST))

Abstract

Ferroelectric tunnel junction (FTJ) is a promising candidate for future memory technologies and much effort has been put into the understandings of its materials and device properties. However, in view of atomistic first-principles calculations, most studies have been so far limited to the equilibrium limit and the behavior of FTJs under non-equilibrium conditions remains largely unexplored. Herein, we describe the first-principles framework that enables the analysis of FTJs under non-equilibrium conditions, which is based on the multi-space constrained-search density functional theory (MS-DFT) formalism we have developed over the years. The unique strength of MS-DFT is that the non-equilibrium free energy as well as electric field-dependent polarization and capacitance can be obtained in a first-principles manner. As an application example, for a representative $SrRuO_3$-$BaTiO_3$-$SrRuO_3$ (SRO-BTO-SRO) FTJ capacitor model, we compute the current density-voltage characteristics and tunneling electro-resistance, and the impact of polarization orientation on the resistance state.

Paper 5.3

11:20AM-11:40AM

Advanced Ferroelectric Modeling for BEOL Negative Capacitance Nanoelectromechanical Switches

Collin Finnan (Electrical Engineering and Computer Science Department, University of California, Berkeley), Lars Tatum (Electrical Engineering and Computer Science Department, University of California, Berkeley) and Tsu-Jae King Liu (Electrical Engineering and Computer Science Department, University of California, Berkeley)

Abstract

Negative capacitance (NC) has been proposed as a means of reducing the pull-in voltage of a nano-electro-mechanical (NEM) switch without physically scaling the device. Existing NC NEM analyses model ferroelectrics assuming a single-domain; however, real devices have multiple antiparallel domains. This work presents a two-dimensional simulation framework for NC NEM switches using two contemporary multi-domain modeling techniques of ferroelectric hafnium zirconium oxide. Though single-domain ferroelectric models result in a dramatic reduction in pull-in voltage, multi-domain models within the same system either do not exhibit NC, or only exhibit limited benefit from the NC effect.

Paper 5.4

11:40AM-12:00PM

Revealing the Noise Dependent Sensitivity of a Junctionless FinFET-based Hydrogen Sensor with Ferroelectric Gate Stack

Navneet Gandhi (PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur), Sunil Rathore (PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur), Rajeewa Kumar Jaisawal (PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur), P N Kondekar (PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur), Naveen Kumar (University of Glasgow), Ankit Dixit (University of Glasgow), Vihar Georgiev (University of Glasgow) and Navjeet Bagga (Indian Institute of Technology Bhubaneswar)

Abstract

This paper presents simulation of a three-dimensional ferroelectric NAND memory using a multi-domain Ginzburg–Landau–Khalatnikov polarization model. The model parameters with a variation range following a Gaussian function are calibrated based on experimental polarization-electric field hysteresis for undoped and 5 mol% Al-doped HfO2 thin films. The allowed memory window between program and erase states can be enlarged from 2.9 to 12.6V through the incorporation of Al dopant in HfO2. This polarization enhancement by substituting Hf with Al atom is also justified through atomistic simulation.

Breakout Session 6 | Sensors & Optoelectron

Sainte Claire Ballroom | 10:10AM-12:00PM

Invited Talk

10:10PM-10:40AM

Approaches to Simulating Meta-surfaces for Flat Optical Devices: The Transition to Solutions Based on Neural Networks

Denis Rideau, Mathys Le Grand, Loumi Tremas, Louis Henri Fernandez-Mouron, Valerie Serradeil, Damien Maitre, Bruce Ray, James Dowinng, Pascal Urard, Habib Mohamad and Enrico Carnemolla

Paper 6.1

Impact of Ion Energy and Yield in Oblique Ion Beam Etching Process for Blazed Gratings

10:40PM-11:00PM

Tobias Reiter (TU Wien, Institute for Microelectronics), Alexander Toifl(Silvaco Europe Ltd.), Sung Won Kong (Silvaco Inc.), Andreas Hössinger (Silvaco Europe Ltd.) and Lado Filipovic (TU Wien, Institute for Microelectronics)

Abstract

We present a model for oblique ion beam etching (IBE) processes which are applied in the fabrication of optoelectronic devices, such as blazed gratings. Our model combines top-down Monte Carlo flux calculation and the Level-Set method to accurately capture the intricate etch profile evolution during the IBE process. We demonstrate the capability of our model by reproducing experimental etch profiles presented by Zhang et al. Furthermore, we study the impact of ion energy and yield on the time evolution of etch profiles, highlighting their crucial roles in shaping the final device geometries.

Paper 6.2 — 11:00PM-11:20PM

Modeling Next Generation Sensor Chips: Towards Predictive Band Structure Models for Quarternary III-V Semiconductor Alloys

Angus Gentles (ams-OSRAM), Mohammed Dehghani (Technical University of Vienna), Rainer Minixhofer (ams-OSRAM), Pedram Khakbaz (Technical University of Vienna), Dominic Waldhoer (Technical University of Vienna) and Michael Waltl (Technical University of Vienna)

Abstract

In this work, an ab initio scheme based on the DFT+U method is presented to model the electronic structure of ternary/quaternary semiconductor alloys. Within this method, optimal sets of Hubbard-U parameters are found for each binary compound of the alloy using a Bayesian optimization scheme. We introduce two interpolation schemes for the U parameters to describe the electronic structure in alloy supercells. By applying them on InGaAsSb we show that their predicted bandgap bowing is much closer to experimental data compared to results based on the virtual crystal approximation. The two schemes are shown to predict almost identical electronic bandgaps and provide a computationally efficient alternative to other approaches like the use of hybrid functionals.

Paper 6.3 — 11:20PM-11:40PM

Atomistic analysis on random telegraph noise of source follower transistors in sub-micrometer CIS pixels

Jae Ho Kim (Samsung Electronics), Sungchul Kim (Samsung Electronics), Hong-Lae Park (Samsung Electronics), Gijae Kang (Samsung Electronics), Seonghoon Ko (Samsung Electronics), Jongsu Yoon (Samsung Electronics), Wook Lee (Samsung Electronics), Yonghee Park (Samsung Electronics), Jonghyun Go (Samsung Electronics), Hyunchul Kim (Samsung Electronics) and Dae Sin Kim (Samsung Electronics)

Abstract

Physical modeling of random telegraph noise (RTN) on L-shaped source follower (SF) transistors in 0.5µm CMOS image sensor (CIS) pixels is conducted, considering discretized traps at the Si/SiO2 interface using density functional theory (DFT). Investigation of the image signal spectrum caused by RTN via measurement are performed. Additionally, the origins of the effect of Fluorine implantation (F-IIP) passivation in the image sensor are discussed from an atomistic perspective.

Paper 6.4 — 11:40PM-12:00PM

Understanding the dynamic perturbative behaviour of Electrolyte-Gated FET based Biosensor with Immobilized Nanoparticles

Naveen Kumar (University of Glasgow), César Pascual García (Luxembourg Institute of Science and Technology), Ankit Dixit (University of Glasgow) and Vihar Georgiev (University of Glasgow)

Abstract

In this study, we introduce a novel methodology to investigate and model the nonlinear perturbative behavior in Electrolyte-Gated Field-Effect Transistor (EGFET) based biosensors that are enhanced with immobilized nanoparticles. Our approach systematically addresses the perturbations due to redundant silanol sites by quantifying their impact on sensor output, thereby improving the reliability of the sensor readings. Additionally, we explore the role

of neutral gold nanoparticles in augmenting the sensor's ability to detect and differentiate amino acid fingerprints effectively. Moreover, our research delves into the effects of random partial hybridization of carboxylic acids (amino acids) under varying conditions, which alter the reactive sites available for binding. By integrating these factors into our analysis, we provide a robust framework for calibrating and benchmarking experimental data.

Breakout Session 7 | Memory

Grand Ballroom | 1:00-3:00PM

Paper 7.1

1:00PM-1:20PM

A Multiscale Simulation Approach for Program Noise and Cross-temperature Effects in 3D NANDs

Keng-Hua Lin (Synopsys), Salvatore Maria Amoroso (Synopsys), Po-Chou Chen (Synopsys), Yueh-Ying Tseng (Synopsys), Andrew Robert Brown (Synopsys), Plamen Asenov (Synopsys), Ulrik Vej-Hansen (Synopsys), Xi-Wei Lin (Synopsys), Victor Moroz (Synopsys), Chih-Chiang Wang (Synopsys) and Anders Blom (Synopsys)

Abstract

NAND technology keeps reaching unprecedented levels of bit density, mainly thanks to 3D stacking – with most players delivering today more than 200 layers in a four-bit-per-cell technology. With densities of billions of cells per chip, variability from both process variations and intrinsic statistical variations becomes a fundamental design concern. Moreover, the polysilicon channel material adopted in 3D NANDs adds new reliability aspects to the cross-temperature effect. This issue appears when the NAND memory is read at a different temperature from that at which it was programmed. This was previously known in 2D NANDs, but 3D NANDs exacerbate this effect because the polysilicon trap occupancy (and the associated variability) is modulated by the temperature. Numerical simulation is a powerful tool to investigate such phenomena. However, the variability response to temperature depends on the trap energy distributions in the polysilicon bandgap, which is typically approximated by empirical distributions and calibrated to hardware data. In this paper, for the first time to the best of our knowledge, we obtain a deeper physics-based understanding of polysilicon grain boundaries and its defects by ab-initio simulations. We then use ab-initio-calculated trap properties to inform 3D TCAD, paving the path to a multiscale approach to the statistical simulation of 3D NAND cells.

Paper 7.2

1:20PM-1:40PM

Modeling the Operation of Charge Trap Flash Memory: A Monte Carlo Approach to Carrier Distribution and (De)Trapping

Thomas Hellemans (imec + KU Leuven), Devin Verreck (imec), Antonio Arreghini (imec), Geert Van den Bosch (imec), Maarten Rosmeulen (imec), Michel Houssa (KU Leuven + imec) and Jan Van Houdt (imec + KU Leuven)

Abstract

We propose a Monte Carlo framework including (de)trapping to describe the non-equilibrium operation of charge trap flash memories. We thereby base the empirical carrier distribution that was proposed in recent studies on physical parameters. After an outline of the simulation procedure, we show how carrier trapping and detrapping is included. Finally, we illustrate the simulators' capabilities via simulations of the programming and retention operations, highlighting the insight into the carrier dynamics that this approach enables.

Paper 7.3 1:40PM-2:00PM

D2D Variation Aware DTCO for Novel Vertical a-IGZO-FETs in Large-Scale M3D 2T0C DRAM Bit Cell Evaluation via Statistical Modeling Methodology

Yue Zhao (Institute of Microelectronics of the Chinese Academy of Sciences), Yong Yu (Beijing Superstring Academy of Memory Technology), Jingrui Guo (Institute of Microelectronics of the Chinese Academy of Sciences), Lingfei Wang (Institute of Microelectronics of the Chinese Academy of Sciences), Nan Yang (Beijing Superstring Academy of Memory Technology), Jianpeng Jiang (Beijing Superstring Academy of Memory Technology), Yanan Lu (Beijing Superstring Academy of Memory Technology), Menglong Zhou (Beijing Superstring Academy of Memory Technology), Shijie Huang (Institute of Microelectronics of the Chinese Academy of Sciences), Lihua Xu (Institute of Microelectronics of the Chinese Academy of Sciences), Zhenhua Wu (Institute of Microelectronics of the Chinese Academy of Sciences), Guanhua Yang (Institute of Microelectronics of the Chinese Academy of Sciences), Di Geng (Institute of Microelectronics of the Chinese Academy of Sciences), Guilei Wang (Beijing Superstring Academy of Memory Technology), Bryan Kang (Beijing Superstring Academy of Memory Technology), Chao Zhao (Beijing Superstring Academy of Memory Technology), Ling Li (Institute of Microelectronics of the Chinese Academy of Sciences) and Ming Liu (Institute of Microelectronics of the Chinese Academy of Sciences).

Abstract

Device nonuniformity of ultra-scaled novel vertical a-IGZO-FETs is induced by multi-sources, such as dimension variation and material disorder, limiting large-scale DRAM design. Particularly, fluctuation of disorders in an amorphous channel exhibits a great impact on density of states (DOS) contributing to statistical effects on gate controllability and transport mechanisms. To clarify this issue, TCAD simulations are conducted by adjusting geometric dimensions and DOS, and corresponding statistical characteristics (e.g., on-voltage and on-current etc.) are extracted from up to 80 samples of down to channel length of 50nm. Such effects are further incorporated into a surface-potential based physics compact model via calibration to experiments. Using this model, the vertical a-IGZO-FET-based 2T0C DRAM is firstly investigated with the statistical analysis of Write/Read performances, supporting device variation aware DTCO flow of future extremely large-scale and high-density M3D memory.

Paper 7.4 2:00PM-2:20PM

Modeling Row Hammer Effect in 3D Capacitor-less DRAM using Triple-Gated Silicon Nanosheet Device

Jimin Son (Pukyong National University), Jun Young Park (Pukyong National University), Taeeun Lee (Pukyong National University), Sola Woo (Pukyong National University) and Shimeng Yu (Georgia Institute of Technology)

Abstract

A monolithically stackable 3D capacitor-less DRAM structure using triple-gated silicon nanosheet device is demonstrated using TCAD simulation. Our proposed device exhibits a low programming voltage of 1.8 V, a high current sense margin of 78 μA, a fast speed of 5 ns and a data retention time of more than 104 s. In addition, we evaluate the row hammer effect on the 3D array level, including program, erase, read, and hold operations. The simulation results show a robust storage node potential despite repeated attack operations from the neighboring cell.

Paper 7.5 — 2:20PM-2:40PM

Electrical TCAD Simulation of STT-MRAMs

Hanane Chems Saifi(Aix-Marseille Univ, CNRS, IM2NP), Jérémy Postel-Pellerin (Aix-Marseille Univ, CNRS, IM2NP), Nicole Yazigy (Aix-Marseille Univ, CNRS, IM2NP), Noémie Couzi (Aix-Marseille Univ, CNRS, IM2NP), Vincenzo Della Marca (Aix-Marseille Univ, CNRS, IM2NP), Pierre Canet (Aix-Marseille Univ, CNRS, IM2NP), Nuno Caçoilo (SPINTEC, University Grenoble Alpes, CNRS, CEA-SPINTEC, CEA), Grégory Di Pendina (SPINTEC, University Grenoble Alpes, CNRS, CEA-SPINTEC, CEA) and Ricardo C. Sousa (SPINTEC, University Grenoble Alpes, CNRS, CEA-SPINTEC, CEA)

Abstract

In this paper, we propose to develop a full TCAD simulation, using a commercial tool (Sentaurus), of an STT- MRAM device to better understand its electrical behavior. To our knowledge, it is the first time that a simulated I-V hysteresis loop is calibrated on experimental data. The impact of several key parameters is presented, and the obtained values are in good agreement with the ones found in literature. This calibrated TCAD simulation can then be used to study the variability of the switching voltages and the impact of process variations.

Breakout Session 8 | Machine Learning/AI Based Modeling

Sainte Claire Ballroom | 1:00PM-3:00PM

Paper 8.1 — 1:00PM-1:20PM

STEM Image Based Structure Generation for Advanced CMOS Devices

Felix Widauer (Global TCAD Solutions GmbH), Xaver Klemenschits (Global TCAD Solutions GmbH), Cedrik Balla (Global TCAD Solutions GmbH), Gerhard Rzepa (Global TCAD Solutions GmbH), Jose Maria Gonzalez-Medina (Global TCAD Solutions GmbH), Bonny Dongre (Global TCAD Solutions GmbH), Georg Strof (Global TCAD Solutions GmbH), Zlatan Stanojevic (Global TCAD Solutions GmbH) and Markus Karner (Global TCAD Solutions GmbH)

Abstract

Process technology computer aided design (TCAD) has become an indispensable tool to characterize proposed technologies, however current solutions often require tedious manual calibrations of process flows. Here, we present the automatic processing of electron microscopy (EM) images to 2D and 3D device representations. Parts of the device which are not present in the EM image are emulated to create a structure ready for device simulation. The feasibility of this approach is shown by extracting the fin shape from the EM image of a 7 nm FinFET, as well as studying the impact of fin shape on device characteristics in an exemplary variability study. Additionally, the inner spacers and gate shape of a nanosheet (NS) FET are reproduced, showcasing the versatility of the presented approach.

Paper 8.2 — 1:20PM-1:40PM

Equipment-Informed Machine Learning-Assisted Feature-Scale Plasma Etching Model

Lado Filipovic (CDL for ProMod at the Insistute for Microelectronics, Technische Universität Wien), Tobias Reiter (CDL for ProMod at the Insistute for Microelectronics, Technische Universität Wien), Julius Piso (Insistute for Microelectronics, Technische Universität Wien) and Roman Kostal (Insistute for Microelectronics, Technische Universität Wien).

Abstract

We investigate means to merge feature-scale and reactor-scale models during plasma etching using machine

learning (ML) and interpolative approaches. First, we test the SF6/O2 plasma etching models based on a small dataset from literature. We find that Gaussian process regression (GPR) leads to significant over-fitting, resulting in waviness in the predicted values in the range where no data is available. A neural network (NN) model was likewise implemented with rectified linear unit activation. This model provides linear prediction between known values, resulting in a better qualitative fit to experimental observations. Finally, we perform about 19,000 chamber simulations of a Cl2/Ar plasma while varying relevant input parameters. The data is used to build an inerpolative model of the chamber and provide a means to quickly extract relevant fluxes for the feature-scale model

Paper 8.3 1:40PM-2:00PM

A SPICE-compatible Neural Network Compact Model for Efficient IC Simulations

Chien-Ting Tung (UC Berkeley), Sayeef Salahuddin (UC Berkeley) and Chenming Hu (UC Berkeley)

Abstract

We present a SPICE-compatible neural-network-based compact model for advanced FETs. The model consists of an IV and QV network which have all terminal currents and charges and includes geometry dependence. The study of the activation functions is conducted to find the most efficient function for circuit simulations. The model is then implemented in Verilog-A with direct multiplication instead of loops to enhance the computational speed. We demonstrate and benchmark the neural network model performance in large circuit simulations with different network structures. It shows about 40 times speed improvement compared to the conventional compact model.

Paper 8.4 2:00PM-2:20PM

FuncAnoDe: A Function Level Anomaly Detection in Device Simulation

Tae Il Oh (Alsemy Inc.), Hong Chul Nam (Alsemy Inc., ETH Zurich), Chanwoo Park (Alsemy Inc.), and Hyunbo Cho (Alsemy Inc.)

Abstract

In semiconductor device simulations, the reliance on empirical compact models, such as the Berkeley Short-channel IGFET Model (BSIM) and neural compact models, introduces approximations that may significantly diverge from actual physical phenomena. Identifying and filtering out unphysical behaviors and erroneous simulation outcomes is a challenging task, traditionally requiring extensive expert involvement and incurring high costs. In response, we introduce FuncAnoDe, a deep learning network for unsupervised functional anomaly detection in semiconductor simulation datasets. FuncAnoDe is the first to offer deep learning based function-level anomaly detection without the need for manual expert intervention. Its function-level encoder decoder architecture enables application across a diverse range of device parameters and simulations, ensuring scalability and high accuracy in identifying physically implausible parameter configurations. Our evaluations conducted through complex capacitance-voltage (C-V) curve analysis, confirming FuncAnoDe's effectiveness in anomaly detection, achieving a 100.00% accuracy rate without reliance on manual labeling. FuncAnoDe's contribution is in providing a methodological advancement that enhances the precision, reliability, and efficiency of semiconductor design and simulation workflows.

Paper 8.5 2:20PM-2:40PM

TCAD Structure Input File Generation Using Large Language Model

Le Minh Long Nguyen (San Jose State University), Albert Lu (San Jose State University), and Hiu Yung Wong (San Jose State University)

Abstract

Large Language Models (LLMs) such as ChatGPT have been revolutionizing various fields from education to medicine. LLMs are machine learning models trained on vast amounts of text data from the Web and are designed to understand, generate, and interact with humans through natural languages such as English. TCAD, as a sophisticated engineering tool, usually requires a significant amount of expertise from the engineers to set up an appropriate structure. It is thus desirable to train LLMs which can generate input files for structure generation based on natural languages. However, unlike programming languages such as Python which have abundant training examples on the Web, TCAD examples are scarce. In this work, using TCAD Sentaurus Structure Editor (SSE) as an example, 2000 nanowire data are generated to fine-tune Llama 2 (an open-source LLM developed by Meta [1]) to obtain a chatbot that can generate an SSE input file for a nanowire with 18 parameters with English as an instruction. Structures are then created using SSE to verify the correctness of the input files. It should be noted that although the chatbot is limited to nanowire generation, only 2k training data is required (note that 218 ~ 262k already if a full factorial design of experiment is needed) and it responds accurately to English not seen in the training data. This demonstrates a huge potential to use LLM in TCAD input file generation when more sophisticated fine-tuning data and computing resources are available and the importance of the pre-training Web data.

Fri, September 27th

Breakout Session 11 | Advanced CMOS Logic

Grand Ballroom | 9:00AM-10:30PM

Invited Talk 9:00AM-9:30AM

Advances in Modeling of Interconnect Materials

Blanka Magyari-Kope and Jeff Wu

Paper 11.1 9:30PM-9:50PM

Atomistic Multiscale Simulation-Based Extraction of Design Margins in Advanced Transistor Architectures

Jun Jung (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Geunsang Yoo (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Alexander Schmidt (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Wonyup Song (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Hiroyuki Kubotera (TCAD-lab, Samsung Semiconductor Inc. 3655 N 1st street, San Jose, CA 95134, United States), Muralikrishna Raju (TCAD-lab, Samsung Semiconductor Inc. 3655 N 1st street, San Jose, CA 95134, United States), Byounghak Lee (TCAD-lab, Samsung Semiconductor Inc. 3655 N 1st street, San Jose, CA 95134, United States), Woosung Choi (TCAD-lab, Samsung Semiconductor Inc. 3655 N 1st street, San Jose, CA 95134, United States), Anthony Payet (Process TCAD Lab, Samsung DSRJ, Yokohama Mitsui Building, 1-1-2, Takashima, Nishi-ku,

Yokohama-shi, Kanagawa, Japan), Hiroo Koshimoto (Process TCAD Lab, Samsung DSRJ, Yokohama Mitsui Building, 1-1-2, Takashima, Nishi-ku, Yokohama-shi, Kanagawa, Japan), Yasuyuki Kayama (Process TCAD Lab, Samsung DSRJ, Yokohama Mitsui Building, 1-1-2, Takashima, Nishi-ku, Yokohama-shi, Kanagawa, Japan), Beom Seo Kim (DRAM PA2, Memory, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Chungyeon Lee (DRAM Process Development, Memory, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Jamin Koo (DRAM Process Development, Memory, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Joohyun Jeon (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea), Seungmin Lee (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea) and Dae Sin Kim (CSE Team, Innovation Center, Samsung Electronics, 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do, Korea).

Abstract

Employing Kinetic Monte Carlo (KMC) method for epitaxy simulation reinforced with Molecular Dynamics for KMC model parameter extraction, this study establishes an approach for determining design margins in transistor architectures characterized by high aspect ratio cavities. This integrated atomistic and multiscale simulation framework allows prediction of the epitaxy quality and potential defects as well as the optimization of key design parameters.

Paper 11.2 — 9:50PM-10:10PM

Characteristic Variability of GAA Si NS CFETs Induced by Process Variation Effect and Intrinsic Parameter Fluctuation

Min-Hui Chuang (National Yang Ming Chiao Tung University), Sekhar Reddy Kola (National Yang Ming Chiao Tung University) and Yiming Li (Department of Electrical Engineering, National Chiao-Tung University, 1001 Ta Hsueh Road, Hsinchu 300, Taiwan)

Abstract

We simultaneously estimate the impact of process variation effect (PVE) including three major variation factors and intrinsic parameter fluctuation (IPF) including two key random sources on electrical characteristics of gate-all-around silicon nanosheet complementary field-effect transistors (GAA Si NS CFETs). The combined influence of PVE and IPF on both N-/P-FETs in GAA Si NS CFETs results in significant fluctuation of the off-state current. This variability to PVE factors is particularly pronounced in the P-type device due to the parasitic nature of its bottom channel. Furthermore, compared with the magnitudes of dynamic and short circuit powers, the static power is marginal, but it possesses the largest fluctuation (about RSD of 82%). Notably, the statistical sum of each factors of fluctuation overestimates the total variability owing to ignoring the correlation effects among all random factors, compared with the estimation at the same time.

Paper 11.3 — 10:10PM-10:30PM

Hierarchical Transport Modeling for Path-Finding DTCO

Lee-Chi Hung (Global TCAD Solutions GmbH), Gerhard Rzepa (Global TCAD Solutions GmbH), Markus Kampl (Global TCAD Solutions GmbH), Chen-Ming Tsai (Global TCAD Solutions GmbH), Franz Schanovsky (Global TCAD Solutions GmbH), Oskar Baumgartner (Global TCAD Solutions GmbH), Zlatan Stanojević (Global TCAD Solutions GmbH) and Markus Karner (Global TCAD Solutions GmbH)

Abstract

We present a hierarchical flow for predictive TCAD device simulation in DCTO applications. Using a thoroughly calibrated

sub-band Boltzmann transport equation (SBTE) solver, TCAD device simulation parameters for the technology under investigation are generated automatically. This flow enables predictive accuracy of the SBTE solver at turn-around-times of SPICE simulations. It is demonstrated here for an A14 nanosheet technology, i) showing all intermediate calibration details and ii) highlighting a considerable improvement in the accuracy of ring-oscillator performance.

Breakout Session 12 | Quantum Computing

Sainte Claire Ballroom | 9:00AM-10:30PM

Invited Talk
9:00PM-9:30PM

Hierarchical simulation of monolithic CFETs using atomistic and continuum models

Woosung Choi, Hyeon-Kyun Noh, Hong-Hyun Park, Anh-Tuan Pham, Seonghoon Jin, Byounghak Lee, Chihak Ahn, Hiroyuki Kubotera and Dae Sin Kim

Paper 12.1
9:30PM-9:50PM

Simulation of qubits confined in pseudo magnetic field generated by strained graphene nanoribbon

Yusuke Hayashi (Department of Electrical and Electronic Engineering, Kobe University) and Satofumi Souma (Department of Electrical and Electronic Engineering, Kobe University)

Abstract

We propose a quantum dot device with a pseudo magnetic field generated by strained graphene nanoribbon.The ripple of graphene nanorribon generates the strong pseudo magnetic field with large undulation. We find the Landau levels are formed in the pseudo magnetic field and the double quantum dot is created with the energy difference of tens of meV. The result implies that the tunnel coupling of the double quantum dot can be possibly controlled via the variation of the strain.

Paper 12.2
9:50PM-10:10PM

Rapid Simulation Framework for Superconducting Qubit Readout System Inverse Design and Optimization

Albert Lu (San Jose State University) and Hiu Yung Wong (San Jose State University)

Abstract

Qubit readout is one of the most important operations in quantum computers. In superconducting quantum computers, the success of readout depends on many parameters and is difficult to optimize due to the high dimensionality of the problem. In this work, a rapid simulation framework that comprises an analytical model, a neural network (NN), and optimizers using the NN as a surrogate model is proposed. The analytical model is calibrated to the experimental result and allows rapid simulations to generate enough data to train NNs. Single and multi-objective optimizations are performed. It is shown that a better solution can be found using the optimizer than human optimization. Moreover, the framework can find designs with out-of-the-training-range parameters.

Paper 12.3 10:10PM-10:30PM

Study of Using Variational Quantum Linear Solver for Poisson Equation

Nithin Reddy Govindugar (San Jose State University) and Hiu Yung Wong (San Jose State University)

Abstract

Quantum computing is promising in speeding up the system of linear equations (SLE) solving process. However, its performance is limited by noise. The variational quantum linear solver (VQLS) algorithm is expected to be more resilient to noise than gate-based quantum computing algorithms. This is because error correction is not available yet and VQLS is based on cost function minimization. In this paper, the gate insulator Poisson equation is solved using VQLS. The results are compared to technology computer-aided design (TCAD) results and gate-based quantum algorithm results. We show that, even without error-free qubits, the IBM-Q quantum computer hardware can solve a 2-variable SLE with high fidelity. We further demonstrate that, through VQLS simulation, an 8-variable SLE can be solved with fidelity as high as 0.96.

Breakout Session 9 | Planar CMOS Technology

Grand Ballroom | 10:50AM-11:50PM

Paper 9.1 10:50PM-11:10PM

Modeling and Understanding Threshold Voltage and Subthreshold Swing in Ultrathin Channel Oxide Semiconductor Transistors

Koustav Jana (Stanford University), Shuhan Liu (Stanford University), Kasidit Toprasertpong (University of Tokyo), Qi Jiang (Stanford University), Sumaiya Wahid (Stanford University), Jimin Kang (Stanford University), Jian Chen (Stanford University), Eric Pop (Stanford University) and H.-S. Philip Wong (Stanford University)

Abstract

We present a physics-based model for ultrathin channel oxide semiconductor field-effect transistors (OSFETs) which successfully incorporates and explains several important OSFET physics: (1) threshold voltage dependence on OSFET device parameters such as channel thickness, gate dielectric capacitance, and gate metal work function, and OS material parameters such as electron affinity and channel doping, (2) impact of trap-like localized states due to the amorphous nature of the OS, (3) effect of sub-gap Gaussian states from oxygen vacancies and other point defects, and (4) the importance of enhancing gate control to alleviate the effect of traps on the subthreshold swing and threshold voltage.

Paper 9.2 11:10PM-11:30PM

Cryogenic Modeling of 22nm FDSOI MOSFET

Yihong Qing (ADVISE, KU Leuven, Belgium), Jinghao Zhao (ADVISE, KU Leuven, Belgium), Valentijn De Smedt (ADVISE, KU Leuven, Belgium) and Jeffrey Prinzie (ADVISE, KU Leuven, Belgium)

Abstract

In this work, we introduce a TCAD modeling approach for 22nm ultra-thin body and buried oxide fully depleted silicon on insulator (UTBB-FDSOI) MOSFETs, tailored to operate at cryogenic temperatures ranging from 300 K down to 4.5 K. Incorporating relevant physical effects, this TCAD model is calibrated using experimental data from a test chip.

On-chip bootstrapping is employed to mitigate leakage currents from the device test arrays, ensuring precise low current measurements (in the order of a few nA). Our results provide insight in the behaviour of the threshold voltage, subthreshold swing, and back gate bias effect at cryogenic temperatures, offering valuable guidance for low-power circuits and quantum computing read-out IC design.

Paper 9.3 11:30PM-11:50PM

Improved Compact Modeling of Snapback Behaviour in ESD MOSFETs

Anant Singhal (Indian Institute of Technology Jodhpur), Garima Gill (Indian Institute of Technology Jodhpur), Avinash Lahgere (Indian Institute of Technology Kanpur), Girish Pahwa (International College of Semiconductor Technology, National Yang Ming Chiao Tung University) and Harshit Agarwal (Indian Institute of Technology Jodhpur)

Abstract

In this work, we present an improved physics-based ESD compact model to capture the snapback triggering voltage (Vt1) and the snapback triggering current (It1) which defines the on-set of the ESD protection device. The proposed model is designed to capture snapback behavior in both MOSFETs and HV-MOSFETs, without relying on parameters extracted solely from measurement data. The proposed model is successfully validated through extensive TCAD simulations and experimental data for HV-MOSFETs. The proposed model is simple and can be easily integrated with industry standard compact models.
// Anant Singhal and Garima Gill have equally contributed for this work which has been highlighted in the manuscript.

Breakout Session 10 | Chip-Level & Packaging Modeling

Sainte Claire Ballroom | 10:50AM-11:50PM

Paper 10.1 10:50PM-11:10PM

Full Chip Stress Model for Defect Formation Risk Analysis in Multilayer Structures

Kyungmi Yeom (Samsung Electronics), Geunsang Yoo (Samsung Electronics), Alexander Schmidt (Samsung Electronics), Anthony Payet (Samsung DSRJ), Yutaka Nishizawa (Samsung DSRJ), Masaru Uchiyama (Samsung DSRJ), Yasuyuki Kayama (Samsung Electronics), Chihak Ahn (Samsung Semiconductor Inc), Woosung Choi (Samsung Semiconductor Inc), Joohyun Jeon (Samsung Electronics), Seungmin Lee (Samsung Electronics) and Dae Sin Kim (Samsung Electronics)

Abstract

To overcome the limitations of the previously developed stress simulation method for full-chip scale [1], which could only analyze a single layer of metallization due to its use of a shell element method, a simulation flow that can handle multiple layers was developed. Introducing stress simulation during the incremental formation of the back-end-of-line (BEOL) structure is crucial for predicting the risk of stress-induced defects not just on the surface, but throughout the entire 3D structure, including the chance of defects between metallization layers. To enhance the predictive capability for the larger-scale stress-induced defects, local stress averaging was utilized to balance simulation accuracy with coverage area. This methodology allowed for the expansion of the simulation domain beyond the chip level, thereby enabling the estimation of layout-induced deformations on a wafer scale.

Paper 10.2

11:10PM-11:30PM

Self-consistent tiling method for the chip-scale stress simulation

Chihak Ahn (Samsung semiconductor Inc.), Kyungmi Yeom (Samsung Electronics), Alexander Schmidt (Samsung Electronics), Yutaka Nishizawa (Samsung Device solutions R&D Japan), Anthony Payet (Samsung Device solutions R&D Japan), Seonghoon Jin (Samsung Semiconductor Inc.), Yasuyuki Kayama (Samsung Device solutions R&D Japan), Woosung Choi (Samsung Semiconductor Inc.) and Dae Sin Kim (Samsung Electronics)

Abstract

We present a self-consistent boundary treatment method to account for the long-range stress effects in chip-scale stress simulations. The long range effects are superposed onto the stress solution of the individual tiles as the boundary displacements in a self-consistent manner. The model concept is rigorously tested and applied to a realistic example to demonstrate large-scale simulation capability. Chip-scale and even wafer-scale simulations can be achieved by the nested application of the proposed method. An important potential application would be mask design improvement to avoid stress-related device failure.

Paper 10.3

11:30PM-11:50PM

3D Electromagnetic simulation and modeling for DTCO of decoupling high-density capacitor in silicon interposer for HPC applications

Hélène Jacquinot (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France), Emmanuel Pluchart (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France), Frédéric Rothan (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France), Sébastien Martinie (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France), Takuo Wakaoka (Murata Manufacturing Co., Ltd. Kyoto, Japan), Ryo Kasai (Murata Manufacturing Co., Ltd. Kyoto, Japan), Seiji Hidaka (Murata Manufacturing Co., Ltd. Kyoto, Japan), Frédéric Voiron (Murata Integrated Passive Solutions, SAS Caen, France), Cyrille Laviron (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France) and Yasser Moursy (Univ. Grenoble Alpes, CEA, LETI F-38000 Grenoble, France)

Abstract

In this paper, we present a Design-Technology Co-Optimization (DTCO) methodology of a heterogeneous 2.5Dsystem that aims at integrating a passive interposer with HPC chiplets. The interposer comprises 3D high-density decoupling capacitors with the power delivery network (PDN) of the HPC chiplets. The proposed methodology is based on the discretization of the interposer into unit-cells and uses spatially distributed SPICE modeling to achieve voltage drop optimization, thus improving the performance of the chiplets at system level, in iterative loop processes. Using Electromagnetic (EM) simulation for unit-cells, incorporating boundary conditions that can be customized, we found out that neighboring cells play a significant role in the voltage drop seen inside the unit-cell as a result of resistive and inductive distributed parasitic interconnects. Consequently, these adjacent cells were incorporated into the EM simulation set-up for accurate power integrity analysis at system level.

Invited Talks

Wed, September 25th

Breakout Session 1

Grand Ballroom | 10:10AM-10:40AM

Mode space in DFTB quantum transport in the nanodevice simulation tool NEMO5

Logan Melican, Han-Wei Hsiao, Daniel Lemus and Tillmann Kubis

Breakout Session 2

Sainte Claire Ballroom | 10:10AM-10:40AM

Logic DTCO/STCO

Victor Moroz, Synopsys Inc.

Thu, September 26th

Breakout Session 5

Grand Ballroom | 10:10AM-10:40AM

A TCAD to SPICE Simulation Framework for Analysis of Device to Circuit BTI and HCD Aging

Payel Chatterjee, Karansingh Thakor and Souvik Mahapatra

Breakout Session 6

Sainte Claire Ballroom | 10:10AM-10:40PM

Approaches to Simulating Meta-surfaces for Flat Optical Devices: The Transition to Solutions Based on Neural Networks

Denis Rideau, Mathys Le Grand, Loumi Tremas, Louis Henri Fernandez-Mouron, Valerie Serradeil, Damien Maitre, Bruce Ray, James Dowinng, Pascal Urard, Habib Mohamad and Enrico Carnemolla

Thu, September 26th

Breakout Session 11

Grand Ballroom | 9:00AM-9:30AM

Advances in Modeling of Interconnect Materials

Blanka Magyari-Kope and Jeff Wu

Breakout Session 12

Sainte Claire Ballroom | 9:00AM-9:30AM

Hierarchical simulation of monolithic CFETs using atomistic and continuum models

Woosung Choi, Hyeon-Kyun Noh, Hong-Hyun Park, Anh-Tuan Pham, Seonghoon Jin, Byounghak Lee, Chihak Ahn, Hiroyuki Kubotera and Dae Sin Kim

Poster Papers Submissions

Poster 1
Chip Reliability Improvement by Designing Re-Distribution Layer (RDL) Pattern for Thermal Cycle in Wafer Level Packages (WLP)

Sora Park (Samsung Electronics Co., Ltd), Donggwan Shin (Samsung Electronics Co., Ltd), Yonghee Park (Samsung Electronics Co., Ltd) and Dae Sin Kim (Samsung Electronics Co., Ltd)

Abstract
We investigate the re-distribution layer (RDL) design effect on the Vref, the output voltage of band gap reference (BGR) circuit, during the reliability test by temperature cycling (TC). The TC failure mechanism is analyzed using TCAD simulation and verified with the experimental data. We reveal that the mechanical stress of deposited polyimide between RDL films during TC can influence the device performance. The local stress caused by RDL patterns induces the mismatch between the transistors in relations of the current mirroring in BGR circuit and the Vref can shifted. Therefore, for reliability of the chip performance in wafer level package (WLP), we should consider the position of the stress-sensitive circuits such as BGR when designing the RDL.

Poster 2
Neural Drift-Diffusion Model Based on Operator Learning in Fourier Space

Kyeyeop Kim (Computational Science and Engineering Team, Innovation Center, Samsung Electronics), Sanghoon Myung (Computational Science and Engineering Team, Innovation Center, Samsung Electronics), Yunji Choi (Computational Science and Engineering Team, Innovation Center, Samsung Electronics), Gijae Kang (Computational Science and Engineering Team, Innovation Center, Samsung Electronics), Songyi Han (Computational Science and Engineering Team, Innovation Center, Samsung Electronics), Jaehoon Jeong (Computational Science and Engineering Team, Innovation Center, Samsung Electronics) and Dae Sin Kim (Computational Science and Engineering Team, Innovation Center, Samsung Electronics)

Abstract
Using a microscopic picture of atomic movement we rederived the Fick's diffusion flux equation which naturally includes all types of drift terms (e.g. electrical drift, stress driven movement, and binding energy related effects). With a similar method, two phase segregation transfer rate and three phase segregation trapping/emission rates are also defined with measurable or calculable quantities.

Poster 3
Real Time TCAD Calibration via Transfer Learning

Yunji Choi (Samsung Electronics), Sanghoon Myung (Samsung Electronics), Kyeyeop Kim (Samsung Electronics), Gijae Kang (Samsung Electronics), Beomwon Jeong (Samsung Electronics), Yongwoo Jeon (Samsung Electronics), Songyi Han (Samsung Electronics), Jaehoon Jeong (Samsung Electronics) and Dae Sin Kim (Samsung Electronics)

Abstract
This study introduces a novel calibration framework of deep learning model, called Real Time TCAD (RTT) calibration. The proposed method consists of two steps: pre-training and transfer learning. In the pre-training step, a deep learning

model is trained with uncalibrated TCAD data to learn semiconductor physics. In the transfer learning step, the pre-trained model is finetuned with measurements to close the discrepancy between the model and the measurements. The proposed method can significantly reduce both calibration and data generation time while maintaining high model accuracy. In addition, our method tackles the critical problems that some of data contain missing values in practice. The results of experiments on a 28-nm logic process demonstrate the effectiveness of the proposed method.

Poster 4
Atomistic Simulations of the Impact of Rotational Twin Planes Defects on the Optical Properties of InP Systems

Christian Dam Vedel (University of Glasgow) and Vihar Georgiev (University of Glasgow)

Abstract

Integration of III–V's materials into the current silicon platform usually yields a large number of crystal defects due to a lattice mismatch between the silicon substrate and the III–V materials. A significant amount of research has been performed to investigate how to avoid the formation of defects, such as threading dislocations or rotational twin planes (RTPs). Usually, defects in any materials constituting a device lead to a degradation of the device performance. However, if the defects can be controlled, they can potentially be beneficial for the device performance by enhancing key figures of merit, such as drive current and optical absorption. Hence, in this paper, we explore the possibility of using defects, such as RTPs, in bulk InP material to improve device characteristics, such as photo absorption.

Poster 5
Calibration Insights of Phosphorus Diffusion Model for NMOS FDSOI : Pathway to advanced technology nodes

Anne-Sophie Royet (CEA-LETI), Rihab Chouk (CEA-LETI), Olga Cueto (CEA-LETI), Joel Kanyandekwe (CEA-LETI), Valérie Lapras (CEA-LETI), Marie-Anne Jaud (CEA-LETI), Sébastien Martinie (CEA-LETI), Tadeu Mota-Frutuoso (CEA-LETI), Zdenek Chalupa (CEA-LETI), Olivier Rozeau (CEA-LETI) and Bledion Rrustemi (CEA-LETI)

Abstract

This paper evaluates the lateral dopant diffusion for source and drain junction profiles of NMOS FDSOI devices. Parameters of the phosphorus diffusion model in an in-situ doped epitaxial Source/drain are calibrated using TCAD simulations, and validated against experimental data, which vary with spike anneal temperatures, epitaxy concentrations, and gate lengths. After carefully adjusting these parameters, we incor-porate them into a global simulation approach for device scaling. This enables the transition from current baseline FDSOI technology to even advanced FDSOI technology nodes.

Poster 6
Diffusion-Based Machine Learning Method for Accelerating Quantum Transport Simulations in Nanowire Transistors

Preslav Aleksandrov (University of Glasgow), Pranav Acharya (University of Glasgow) and Vihar Georgiev (University of Glasgow)

Abstract
In this work, we have developed a new TCAD approach based on diffusion-based machine learning (ML) models that combine a latent diffusion model with our existing Non-Equilibrium Green's Function (NEGF) simulator, implemented in our in-house Nano Electronics Simulation Software (NESS). Our results demonstrate the potential of using a diffusion-based extension of the ML-NEGF methodology to substantially reduce the computational cost of device simulations without compromising the accuracy of the physical results.

Poster 7
Modeling of SOI-MOSFET with Trap-Rich Substrate for RF Circuit Design

Soumajit Ghosh (Hiroshima University), Mitiko Miura-Mattausch (Hiroshima University), Hideyuki Kikuchihara (Hiroshima University), Takahiro Iizuka (Hiroshima University), Samir Chaudhry (Tower Semiconductor) and Yasuyuki Sahara (Tower Partners Semiconductor Co., Ltd.)

Abstract
Many efforts have been undertaken to reduce the substrate-coupling effect in RF circuits. It has been demonstrated that a trap-rich layer underneath the BOX can reduce drastically undesired harmonic dis-tortions (HDs), thus maintaining desired signal integrity. To utilize this technology, a newly developed compact model considers the trap charge based on its physics and is implemented into HiSIM_SOI, which solves the whole potential distribution within the device iteratively. The Fermi energy modeling as a function of trap density (Ntrap) is one of the keys for the achieved consistent modeling. It is also demonstrated that the trap charge improves the linearity of the induced potential characteristics during device operation, resulting in a HD reduction.

Poster 8
DTCO of advanced FDSOI CMOS technology by process emulation

Aicha Boujnah (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble), Olga Cueto (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble), Marie-Anne Jaud (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble), Sebastien Martinie (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble), Franck Nallet (Synopsys Switzerland LLC, Thurgauerstrasse 40, Airgate Building, CH-8050 Zurich), Claire Fenouillet-Beranger (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble) and Olivier Rozeau (Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble)

Abstract
This paper presents a methodology of DTCO (DesignTechnology Co-Optimization) for advanced FDSOI CMOS technology based on process emulation. By combining process emulation for the generation of 3D structures, TCAD and SPICE simulations, integrated circuit (IC) performance can be estimated. This work, based on realistic devices taking into account integration flow and interconnects topologies (multilayer dielectrics, contact etching form, etc.) offers a large range of technological and device parameters study. We illustrate the interest of this approach by specifically studying the effect of interconnect oxides permittivity on the performance of a ring oscillator (RO).

Poster 9
A Finite Element Framework for Solving the Density-Gradient Model

Pengcong Mu (Institute of Microelectronics, Chinese Academy of Sciences), Tao Cui (Academy of Mathematics and Systems Science, Chinese Academy of Sciences), Lijun Xu (Institute of Microelectronics, Chinese Academy of Sciences), Kun Luo (Institute of Microelectronics, Chinese Academy of Sciences), Zhiqiang Li (Institute of Microelectronics, Chinese Academy of Sciences) and Zhenhua Wu (School of Pyhsics, Zhejiang University, Institute of Microelectronics, Chinese Academy of Sciences)

Abstract

This paper presents a positive-preserving, stable finite element scheme for the density-gradient (DG) model. An efficient Newton-Krylov solver is designed to address the nonlinear coupled discrete system. Simulation results for gate-all-around (GAA) devices demonstrate the robustness and effectiveness of the proposed scheme. Notably, the simulation time using our method is only half that of the Sentaurus Device, highlighting its superior computational efficiency.

Poster 10
First Simulation of the Effects of Metal Sidewall Source/Drain and Channel Number on the Output Characteristics of Current Mirror Formed by Vertically Stacked GAA Si NS MOSFETs

Kuan-Ju Chou (National Yang Ming Chiao Tung University) and Yiming Li (National Yang Ming Chiao Tung University)

Abstract

In this work, we study the effect of metal sidewall (MSW) source/drain (S/D) on current mirror (CM) formed by vertically stacked gate-all-around (GAA) nanosheet (NS) for the first time. Performance of CM with (w/) and without (w/o) MSW S/D is explored by using a 3D numerical device-circuit simulation. Electrostatic potential distribution in the explored CM changes significantly because of parasitic resistance. The CM w/ MSW S/D reduces the parasitic resistance and has great influence on the output characteristics depending on the CM channel number.

Poster 11
Global Field Heterograph Neural Networks for Accelerating Quantum Transport Calculation

Xiaoxin Xie (School of Integrated Circuits, Peking University), Zhijiang Wang (School of Integrated Circuits, Peking University), Yuchen Wang (School of Integrated Circuits, Peking University) and Fei Liu (School of Integrated Circuits, Peking University)

Abstract

In this work, we propose an attention-based global field heterograph neural network (GFGNN) to characterize field effects and dynamics for the open system. Based on the heterograph abstracted from the device physics, the GFGNN has been verified to have strong predictive power on 2D MoS2 DG-MOSFET, with MAE(mean absolute error) as low as 2.69-4.76 meV for potential profile prediction. By incorporating GFGNN into the NEGF computing framework, an acceleration of 68.18-478.57% can be achieved while maintaining the accuracy of transport property calculations by reducing or even skipping self-consistent iterations. The GFGNN-based method for transport computation extends the research paradigm of data-driven scientific discovery from the field of DFT to NEGF, which will greatly facilitate the exploration and discovery of new materials and devices in the future.

Poster 12
Automated Algorithmic Parameter Extraction of TCAD-Based SPAD SPICE Models

Patryk Maciazek (Univeristy Of Glasgow), Isobel Nicholson (STMicroelectronics Edinburgh), Jean-Robert Manouvrier (STMicroelectronics Crolles), Denis Rideau (STMicroelectronics Crolles), Filip Kaklin (STMicroelectronics Edinburgh), Vihar Georgiev (University Of Glasgow), Elsa Lacombe (‡STMicroelectronics Crolles), Mohammed El-Rawhani (STMicroelectronics Edinburgh) and Christel Buj (‡STMicroelectronics Crolles)

Abstract
We present a methodology of automated parameter extraction for TCAD SPAD SPICE models using the Levenberg-Marquardt algorithm. The demonstrated solution has been validated on a large number of SPAD designs. These have been simulated using a well calibrated process and device simulator. This method can be applied before silicon characterisation for predictive SPICE models.

Poster 13
Non-equilibrium first-principles simulations of TMDC field effect transistors

Seunghyun Yu (Korea Advanced Institute of Science and Technology), Tae Hyung Kim (Korea Advanced Institute of Science and Technology), Juho Lee (Korea Advanced Institute of Science and Technology) and Yong-Hoon Kim (Korea Advanced Institute of Science and Technology)

Abstract
Based on multi-space density functional quantum transport calculations, we perform first-principle based gating simulation for MoS2/metal based two-dimensional (2D) transistors. Our gating method explicitly adopt the atomic model to simulate gate electrode and self-consistently defines gating potential and charge, which differentiates from previous parameter-based method. We find that the p-type band alignment of Ag/MoS2 edge contact is switched to n-type band alignment if gate electrode is introduced. Metal electrode screens the electric field from gate electrode through the channel material, which hinders the gate controllability of the edge-contact junction.

Poster 14
Wafer Edge Profile Integration with 3-D Process Emulation : Model Implementation and Utilization

Jiyong Song (Advanced Analysis Science & Engineering Team, Samsung Electronics.), Wooyoung Cheon (Computational Science and Engineering Team, Samsung Electronics), Yukihide Tsuji (Computational Science and Engineering Team, Samsung Electronics), Yuichiro Higuchi (Process TCAD Lab., Samsung Device Solution R&D Japan), Hisashi Kotakemori (Process TCAD Lab., Samsung Device Solution R&D Japan), Shinwook Lee (Computational Science and Engineering Team, Samsung Electronics), Yasuyuki Kayama (Process TCAD Lab., Samsung Device Solution R&D Japan), Joomi Kim (Advanced Analysis Science & Engineering Team, Samsung Electronics.), Dong Ryul Lee (Advanced Analysis Science & Engineering Team, Samsung Electronics.), Sungho Lee (Advanced Analysis Science & Engineering Team, Samsung Electronics.), Jaehoon Jeong (Computational Science and Engineering Team, Samsung Electronics) and Dae Sin Kim (Computational Science and Engineering Team, Samsung Electronics)

Abstract
Attention has been focused on the front-side surface of the wafer patterning area in the process of developing new semiconductor products. But as the semiconductor process becomes more advanced, process steps increases and

process schemes diversify, attention is required in the areas beyond the front-side as defects and process risks are increasing at the edges and the backside of the wafer. Currently post actions are taken for improvement of defects once they occur at the edges and backside, but through profile simulation of the wafer edge area using the 3D-emulator, we expect to discover the defect risk at an early stage of development before the defect occurs. Hence in this paper, the profile of the wafer edge was implemented using a 3D-emulator, and the consistency with the real profile was confirmed by comparing and analyzing it with the actual wafer profile.

Poster 15
An Improved Overlap Capacitance Model for LDMOS Transistors based on the BSIM-BULK Framework

Ayushi Sharma (Indian Institute of Technology Kanpur), Ahtisham Pampori (UNIVERSITY OF CALIFORNIA BERKELEY), Mingchun Tang (Infineon Technolgies AG Germany), Ravi Goel (Infineon Technolgies AG Germany), Ahmed Mahmoud (Infineon Technolgies AG Germany), Volker Kubrak (Infineon Technolgies AG Germany), Chenming Hu (UNIVERSITY OF CALIFORNIA BERKELEY) and Yogesh Singh Chauhan (Indian Institute of Technology Kanpur)

Abstract
The gate-drain capacitance (CGD) affects the input and output impedance of transistors, necessitating designers to consider it for proper matching and interfacing with other circuit elements. For Laterally Diffused Metal-Oxide-Semiconductor (LDMOS) transistors, the drift region overlap capacitance is a key contributor to CGD. CGD gradually decreases with drain voltage (VD) and eventually saturates. However, before saturating, we observe a stepped decline in CGD at higher VD. This articleprovides physical insights into this step reduction of capacitance using Technology Computer-Aided Design (TCAD) simulations. Using the industry-standard BSIM-BULK model as a framework, we present an improved overlap capacitance model and validate it against measured LDMOS characteristics

Poster 16
Modeling of Trap Generation in 3-D NAND Charge Trap Flash Memory

Anuj Kumar (Indian Institute of Technology Bombay), Ravi Tiwari (Indian Institute of Technology Bombay), Himanshu Rai (Indian Institute of Technology Bombay), Rashmi Saikia (Indian Institute of Technology Bombay), Arnav Shaurya Bisht (Indian Institute of Technology Bombay) and Souvik Mahapatra (Indian Institute of Technology Bombay)

Abstract
The Reaction-Diffusion-Drift (RDD) framework, implemented in both Sentaurus TCAD and standalone 1-D versions, is used to simulate Program/Erase (P/E) cycling related Tunnel Oxide Trap Generation (TO-TG) in Charge Trap Flash (CTF) NAND. The TCAD version uses NAND string as a device structure and bipolar bias for cycling, but is limited in the P/E cycle count due to computational time overhead. The 1-D version has an identical trap generation model as in TCAD, but it uses unipolar pulse for calibration with TCAD bipolar P/E results and extrapolate to high P/E cycle counts. The simulated TO-TG density is incorporated in the Activated Barrier Double Well Thermionic Emission (ABDWT) model to calculate post-cycling data retention (DR) loss. Experimental DR data are reproduced.

Poster 17
Predictive Simulation of Nanosheet Transistors Including the Impact of Access Resistance

Tapas Dutta (University of Glasgow; Semiwise Ltd, Glasgow.), Fikru Adamu-Lema (University of Glasgow; Semiwise Ltd, Glasgow.), Nikolas Xeni (Semiwise Ltd., Glasgow), Ali Rezaei (University of Glasgow), Ankit Dixit (University of Glasgow), Ismail Topaloglu (Semiwise Ltd., Glasgow), Vihar Georgiev (University of Glasgow) and Asen Asenov (University of Glasgow; Semiwise Ltd, Glasgow)

Abstract

In this work we present a hierarchical computational approach to study the impact of source/drain access resistance in nanosheet transistors at the 3nm technology node and beyond. We employ the non-equilibrium Green's function (NEGF) approach to derive the current-voltage characteristics of the nanosheet transistors having extremely short source/drain extensions. Subsequently, we calibrate our quantum-corrected drift-diffusion simulator based on the density gradient formalism, which is then used to simulate structures with realistic lengths of source/drain regions. The device characteristics thus obtained reflect the impact of the access resistance. We analyse the impact of geometry scaling and doping levels in the Source/Drain extensions on the access resistance for different technology nodes.

Poster 18
Density Matrix Based Transport in Heterostructure Devices Utilizing Tight-Binding Approaches

Mathias Pech (TU Dortmund), Alan Abdi (TU Dortmund) and Dirk Schulz (TU Dortmund)

Abstract

By combining a tight-binding solid-state description with an equation of motion for a density matrix defined at the same lattice points, an efficient and atomistic transport model emerges. Instead of mapping the density matrix onto a phase space function like the Wigner function we maintain a real space description, allowing for easy implementation of spatially varying lattice distances and hopping terms. This vastly extends the possible applications of density matrix approaches which on one hand usually require a constant discretization width to perform a Fourier transform and on the other hand usually start from a simple effective mass Hamiltonian. Our approach is applied onto GaAs/Al x Ga 1−x As resonant tunneling diodes and agrees well with stationary results obtained by a quantum transmitting boundary method.

The explicit time-resolved algorithm is shown to converge well and shows great computational efficiency when compared to a Quantum Liouville-type equation. Additionally, the derived equation of motion is well suited for the extension to more complex problems, especially tight binding models that take more neighbors or different orbitals into account.

Poster 19
Modeling of Advanced MRAM Devices for Sub-ns Operation

Bernhard Pruckner (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic, TU Wien), Nils Jørstad (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic, TU Wien), Mario Bendra (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic, Institute for Microelectronics, TU Wien), Tomáš Hadámek (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic, TU Wien), Siegfried Selberherr (Institute for Microelectronics, TU Wien) and Viktor Sverdlov (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic, Institute for Microelectronics, TU Wien)

Abstract
The Reconfigurable Field-Effect Transistor (RFET) enables dual-mode (n-type and p-type) operation in a single device, enhancing circuit design efficiency. However, silicon-based RFETs exhibit low saturation currents, limiting their use in high-performance applications. The Complementary RFET (CRFET) proposed in our previous study inspired by CFET addresses this by merging p-type and n-type RFETs in a stacked layout with dedicated interconnections for source, drain, polarity gate, and control gate. This study introduces the Enhanced CRFET (ECRFET), featuring an optimized Schottky barrier at the source/drain contacts, delivering enhanced performance with low variability at a reduced operation voltage of 0.7V.

Poster 20
Optimization of Complementary Reconfigurable Field-Effect Transistor for Improved Circuit-Level Metrics

Juhan Ahn (The University of Texas at Austin), Saroj Satapathy (The University of Texas at Austin / Intel Corporation) and Jaydeep Kulkarni (The University of Texas at Austin).

Abstract
The Reconfigurable Field-Effect Transistor (RFET) enables dual-mode (n-type and p-type) operation in a single device, enhancing circuit design efficiency. However, silicon-based RFETs exhibit low saturation currents, limiting their use in high-performance applications. The Complementary RFET (CRFET) proposed in our previous study inspired by CFET addresses this by merging p-type and n-type RFETs in a stacked layout with dedicated interconnections for source, drain, polarity gate, and control gate. This study introduces the Enhanced CRFET (ECRFET), featuring an optimized Schottky barrier at the source/drain contacts, delivering enhanced performance with low variability at a reduced operation voltage of 0.7V.

Poster 21
Process Emulation and Device Simulation of Monolithic CFET Inverter and Transmission Gate with Split-gate Structure

Seungwoo Jung (Gwangju Institute of Science and Technology), In Ki Kim (Gwangju Institute of Science and Technology), Kwang-Woon Lee (Gwangju Institute of Science and Technology) and Sung-Min Hong (Gwangju Institute of Science and Technology)

Abstract
In this work, by using an in-house process emulator, the monolithc CFET technology has been considered. Two fabrication options – a conventional common-gate structure and a split-gate structure – are proposed. With the

split-gate structure, a transmission gate, which is essential in realizing the standard logic cells, can be fabricated without any area penalty. Electrical performance of an inverter and a transmission gate is also simulated with an in-house device simulator. The subthreshold swings (SS) of 70.1mV/dec and 69.6mV/dec are obtained for NMOS and PMOS, respectively. The transient simulation results for a transmission gate with 1fF and 0.1fF load capacitances show: τ_{PLH} of 8.45ps and τ_{PHL} of 8.49ps at 1fF, and τ_{PLH} of 5.55ps and τ_{PHL} of 5.52ps at 0.1fF.

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